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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/779,710	02/18/2004	Nobuaki Hashimoto	118355	1715
25944	7590	02/28/2005		
OLIFF & BERRIDGE, PLC P.O. BOX 19928 ALEXANDRIA, VA 22320			EXAMINER EVERHART, CARIDAD	
			ART UNIT 2829	PAPER NUMBER

DATE MAILED: 02/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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<b>Office Action Summary</b>	<b>Application No.</b> 10/779,710	<b>Applicant(s)</b> HASHIMOTO, NOBUAKI	
	<b>Examiner</b> Caridad M. Everhart	<b>Art Unit</b> 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2,9-12 and 14-16 is/are rejected.
- 7) ☒ Claim(s) 3-8 and 13 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |  |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)            |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date ____ | 6) <input type="checkbox"/> Other: ____  |

***Claim Objections***

Claim 15 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 15 is a method claim improperly dependent upon a device claim.

***Claim Rejections - 35 USC § 112***

Claims 10 -12 recite the limitation "the semiconductor substrate" . There is insufficient antecedent basis for this limitation in claim 1 upon which claims 10 and 11 depend, as claim 1 recites "a substrate" rather than a semiconductor substrate.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1,9, 14, 15, and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Iwata, et al. (US 5,512,712).

Iwata, et al discloses a substrate 10 which has electrodes 20 and terminals 20b(col. 4,lines 28-31 and 44-46 and 57-60 and Fig. 1and Fig. 2). The device is a semiconductor device, as it is applied to QPF packaging, which is for semiconductor packaging(col. 2, lines 42-44). The terminals are connected to the electrodes(col. 4,lines 60-62). The electrodes are connected to an integrated circuit through the

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terminals(Fig. 3 and col. 6, lines 40-41). There is a light transmissive insulation layer on the terminal side of the substrate(col. 3, lines 7-10 and 18-20). There is a mark covered by this light transmissible layer which is visible(col. 4, lines 42-52 and col. 5, lines 54-56). The covering layer can be solder resist and the terminal connections can be solder(col. 1, lines 20-26 and col. 6, lines 39-47). The steps in the process of providing the mark, providing an external terminal, and a light transmissive layer are disclosed in the portions of Iwata, et al cited. Providing a mark on one side is interpreted to be the front side of the substrate shown in Fig. 1. The determining the mounting orientation is disclosed in the disclosure that the markings include alignment markings(col. 2,lines 14-18).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 2 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwata et al as applied to claim 1 above further in view of Peterson (US 6,744,144B2).

Iwata et al is silent with respect to the substrate being a semiconductor wafer.

Peterson discloses a wafer 100 with microelectronic dies on the wafer(col. 5, lines 34-40). The substrate can be a wafer made of silicon, glass, or other materials. The dies are integrated circuit dies. (col. 5,lines 38-44).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have used a semiconductor wafer in the device taught by Iwata et al because Iwata et al disclose that the substrate can be glass(col. 5,lines 15-19), and Peterson discloses that silicon can be used instead of glass(col. 5, lines 35-40).

***Allowable Subject Matter***

Claims 3-8 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record does not teach or disclose all of the limitations of the objected to claims, especially ""including at least one land formed on the resin layer" nor "a semiconductor device according to claim 1 mounted thereon".

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Caridad M. Everhart whose telephone number is 571-272-1892. The examiner can normally be reached on Monday through Fridays 7:30-4:00.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C. Everhart  
2-23-2005

*C. Everhart*  
CAROL A. EVERHART  
PRIMARY EXAMINER  
PATENT EXAMINER